VENKATA SRIRAM KAMARAJUGADDA

Portland, OR | +1 (971) 489-6551 | kvsriram06@gmail.com

OBJECTIVE: Internship in VLSI Design Verification/Computer Architecture from Summer (June) 2026.

EDUCATION

MS., Electrical and Computer Engineering **GPA: 3.88/4.0**
Portland State University, Portland, OR (2025-2027)

Courses (By June 2026): SystemVerilog, Pre-Silicon Functional Validation, Microprocessor System Design, System-on-Chip Design with FPGA, Computer Architecture, Hardware for AI & ML.

B.Tech., Electronics and Communication Engineering **GPA: 3.8/4.0**
Jawaharlal Nehru Technological University-MGIT, Hyderabad, TG, India

TECHNICAL SKILLS

- **Programming Languages & Methodologies:** SystemVerilog, UVM, Verilog HDL, C, RISC-V Aseembly, Python.
- **Computer-based tools:** Extensive experience with ModelSim, QuestaSim, Xilinx.
- **Protocols & Architectures:** MESI, RISC-V, MIPS, UART, APB, I2C, DDR.
- **Operating Systems:** Windows, Linux.

TECHNICAL PROJECTS

[UVM] Design Verification of DDR5 PHY (Write Operation): DDR5 PHY write path with command/address logic, write FSM, data shifting, CRC, and register interface. Verified using a class-based UVM testbench, achieving 100% code and functional coverage.

[SystemVerilog] Design and Class-Based Verification of MAC Unit with 3×3 Matrix Multiplication: Parameterized 3×3 MAC architecture with pipelined arithmetic blocks. Verified using a class-based, self-checking testbench with driver, monitor, scoreboard, achieving 100% code and functional coverage.

[SystemVerilog] Design & Class-based Verification of UART Protocol: 8-bit TX/RX, configurable baud rate, start/stop bits, 16× RX oversampling. Verified with UVM-like, Class-based, self-checking testbench with driver, monitor, scoreboard, environment.

[SystemVerilog] Design Verification of Split L1 Cache Controller: Hardware implementation of a split L1 cache with 4-way instruction cache and 8-way data cache, incorporating MESI coherence, LRU replacement, and an inclusive shared L2 interface, verified using a class-based self-checking testbench.

[SystemVerilog] Design Verification of IEEE 754 Floating-point: IEEE 754 single-precision floating-point hardware design with separate modules for exponent alignment, significand addition, sorting, and normalization, verified using a self-checking testbench.

[SytemVerilog] Design & Class-based Verification of APB Protocol: APB-compliant master–slave interface with address, data, and control phases supporting read and write transfers. Verified using Class-based, self-checking testbench with driver, monitor, scoreboard, and protocol checks.

Verilog & SystemVerilog Designs: 4-bit ALU, PISO, FIFO, Single Port RAM, Round Robin Arbiter, Traffic Light Controller, Lift Controller, Wallace Tree Multiplier, Hamming code generator and detector, Sequence Detector.

PROFESSIONAL EXPERIENCE:

Design Verification Intern, Moschip Technologies Limited, Hyderabad: Implemented AMBA APB slave and I2C master/slave modules in Verilog, applying core RTL and hardware modeling techniques. (March – May 2025)

Project Intern, Research Center Imarath-DRDO, Hyderabad: Developed a GPS C/A code generator and key blocks of the parallel code search algorithm, with exploratory integration of acquisition and tracking at the top level. (Oct 2024 – Jan 2025).